What is claimed is:

1. A bias circuit comprising:

a first transistor with a reference voltage coupled to its base terminal;

a second transistor coupled to the emitter terminal of the first transistor at its collector terminal; and,

a third transistor with its base terminal coupled to the first and second transistors, and to an input signal.

2. The bias circuit of claim 1, further comprising a first resistor coupled in series between the emitter terminal of the first transistor and the collector terminal of the second transistor.

3. The bias circuit of claim 1, wherein the input signal comprises a radiofrequency signal.

4. The bias circuit of claim 1, wherein a second reference voltage applied to the base of the third transistor is substantially linear.

5. The bias circuit of claim 1, wherein the quiescent current of the bias circuit is substantially linear.

6. A method for biasing a power amplifier, comprising the steps of:

coupling a reference terminal to a base terminal of a first transistor;

coupling an emitter terminal of the first transistor to at least one device cell of the power amplifier and to a collector terminal of a second transistor; and,

applying a DC reference current at the reference terminal in order to bias the at least one device cell.

7. The method of claim 6, wherein the step of applying a DC reference current comprises applying a current in the range from 10 to 100 microamperes.

8. The method of claim 6, wherein a reference voltage applied to the at least one device cell is substantially linear.

9. A power amplifier circuit comprising:

at least one control circuit coupled to an input terminal;

a power amplifier array coupled to the at least one control circuit; and,

an adder coupled to at least one output of the power amplifier array and coupled to an output terminal,

wherein the power amplifier array further comprises at least one bias circuit, said bias circuit including a first transistor with a reference voltage coupled to its base terminal, a second transistor coupled to the emitter terminal of the first transistor at its collector terminal, and a third transistor with its base terminal coupled to the first and second transistors, and to an input signal.

10. The power amplifier of claim 9, wherein a second reference voltage applied to the base of the third transistor is substantially linear.